## Specification Amendments

Please amend the paragraphs [0005], [0022] and [0023] of the specification as follows:

**[0005]** In static schemes, drivers, repeaters, and receivers are typically simple CMOS static gates, such as inverters. A static scheme may be abstracted in Fig. 2b, where driver **210** and receiver ~~**213**~~ **212** are static inverters. Interconnect **214** may be a large interconnect or large load, for example. Unlike a dynamic scheme, there is no significant power consumption for zero data activity. Furthermore, there is no clocked device that leads to clock power dissipation. However, in contrast to a dynamic scheme, both rising and falling signals received at the input of receiver **212** should be evaluated equally fast. Consequently, it has been desirable in static schemes that receivers should be symmetrical with an inversion threshold in the middle of the power rails. That is, denoting the HIGH and LOW power rail voltages as Vcc and Vss, respectively, the inversion threshold has historically been set at (Vcc-Vss)/2. But for signals with slow edge rates, there may be an undesirable delay before a signal reaches the inversion threshold for a symmetrical receiver. This may result in considerable delay and degrade the performance of a bus.

**[0022]** The operation of the receiver of Fig. 7 is not unlike that of Fig. 3. However, in Fig. 7, the combination of symmetrical inverter **705**, transistors **702** and **704**, and transistors **706** and **708** with their gates connected to the output port of inverter **710**, results in a an asymmetrical inverter with a raised inversion threshold for a rising signal at node **712** and a lowered inversion threshold for a falling signal at node **712**. In

contrast, inverter **312** of Fig. 3 is a symmetrical inverter with fixed inversion threshold. As a result, the variable inversion threshold for the asymmetrical inverter comprising symmetrical inverter **705**, and transistors **702**, **704**, **706**, and **708,** may be designed to ensure that a received signal at input node **712** has made a sufficiently complete transition before the receiver of Fig. 7 is "reconfigured" in favor of the next input signal transition.

**[0023]** Similarly, the operation of the receiver of Fig. 8 is not unlike that of Fig. 6, except that resulting asymmetrical inverter comprising symmetrical inverter **805**, and transistors **802**, **804**, **806**, and **808**, has a raised inversion threshold for a rising signal at node **812** and a lowered inversion threshold for a falling signal at node **812**. As for the receiver of Fig. 7, this ensures that a received signal at input node ~~**812**~~ **712** has made a sufficiently complete transition before the receiver of Fig. 8 is reconfigured in favor of the next input signal transition.